## REMARKS

In response to the Office Action dated October 29, 2003, which was made final, claims 1, 21, and 32 are amended. Claims 1-4, 7, 9, 11, 21-24, 28-30, 31-32, 34-36, 38-40, and 42-63 remain in the application. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Reconsideration of the application, and entrance of these amendments, are respectfully requested.

Art-Based Rejections

In paragraphs 1-2 of the Office Action, claims 1-4, 7, 32, 36, 44-48, 50, and 56-60 were rejected under 35 U.S.C. § 102(e) as being anticipated by Gardner, et al., USPN 6,201,278.

In paragraphs 3-4 of the Office Action, claims 9, 11, 21-24, 28-29, 31, 34-35, 39-40, 42-43, 49-55, and 61-63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner, et al., USPN 6,201,278 in view of Murthy et al., USPN 6,214,679.

The Applicant respectfully traverses the rejections, however, in order to expedite prosecution, the Applicants have amended the claims to clarify the invention. The Applicants respectfully submit that the claims are patentable in light of the amendments above and the arguments below.

The Gardner Reference

The Gardner reference discloses a trench transistor with insulative spacers. The top surfaces of oxide spacers 122A and 122B, oxide segments 126A and 126B, and polysilicon gate electrode130 are aligned and form a planar surface. See Col. 7, lines 33-36.

The Murthy Reference

The Murthy reference discloses a cobalt salicidation method on a silicon germanium film. After the wet etch, monocobalt germano silicide 236 remains on the source/drain regions and on the gate electrode 206 are electrically isolated from each other by the spacers 230 and isolation regions 204. See Col. 8, lines 15-18.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe a semiconductor device. A device in accordance with the present invention comprises a semiconductor substrate having an indented section, a gate dielectric layer disposed on the indented section, a gate electrode disposed on the gate dielectric layer, wherein a portion of the gate electrode is embedded in the semiconductor substrate and another portion of the gate electrode is above the semiconductor substrate, first and second impurity diffusion layers disposed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them, a third impurity diffusion layer disposed in a portion immediately below the gate electrode in the semiconductor substrate, and a sidewall dielectric layer disposed on a side surface section of the gate electrode, wherein the gate electrode has a width that gradually increases from a bottom thereof up to an upper surface thereof, wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, and wherein a majority of the gate electrode and a majority of the sidewall dielectric layer are above the semiconductor substrate, and first and second impurity diffusion layers.

The cited references do not teach nor suggest the limitations of the claims of the present invention. Specifically, the cited references do not teach nor suggest the limitation of a majority of the gate electrode and a majority of the sidewall dielectric layer being above the semiconductor substrate, and first and second impurity diffusion layers as recited in the claims of the present invention.

The Gardner reference discloses a gate electrode higher than the semiconductor substrate, but only by the thickness of the oxide layer. The oxide segments 126A and 126B are thermally grown on substrate 108A and 108B. See Gardner, Col. 7, lines 33-36, where these form a planar surface. As such, the Gardner reference does not teach nor suggest the limitation of a majority of the gate electrode and a majority of the sidewall dielectric layer being above the semiconductor substrate, and first and second impurity diffusion layers as recited in the claims of the present invention.

The Murthy reference does not remedy the deficiencies of the Gardner reference. Namely, the Murthy reference does not teach nor suggest the limitation of a majority of the gate electrode and a majority of the sidewall dielectric layer being above the semiconductor substrate, and first and second impurity diffusion layers as recited in the claims of the present invention.

Since neither reference teaches nor suggest at least one limitation that is present in independent claims 1, 21, and 32, it is respectfully submitted that these claims are patentable over the cited references. Claims 2-4, 7, 9, 11, 22-24, 28-30, 31, 34-36, 38-40, and 42-63 are also patentable over the cited reference, not only because they contain all of the limitations of the independent claims, but because claims 2-4, 7, 9, 11, 22-24, 28-30, 31, 34-36, 38-40, and 42-63 also describe additional novel elements and features that are not described in the prior art.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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